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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,913	05/07/2002	Michael O. Thompson	3672-0144P	8909

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

TH

Office Action Summary	Application No.	Applicant(s)	
	10/088,913	THOMPSON ET AL.	
	Examiner	Art Unit	
	Jung (John) H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 October 2007 has been entered.

2. It is noted that **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). See the Conclusion section below for more details.

Amendment

3. No amendments to the claims have been submitted with the above RCE; therefore, claims 1-18 remain pending in the application, as filed on 23 July 2007.

Claims 6-11 remain withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected invention and species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07 November 2003. It is noted that, because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 13, 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709).

Regarding claims 1, 13 and 17, Kuroda, for example in Figs. 1 and 2, discloses a non-volatile passive matrix memory device comprising ferroelectric memory cells (for example, C0-C7 in Fig. 2); word lines (for example, W00-W07 in Fig. 2) and bit lines (for example, D0-D7 in Fig. 2) that are orthogonal to each other, where each memory cell is at all times in physical contact with a word line and a bit line (for example, in Fig. 2, the memory cell C0 is directly connected to or is directly contacting the word line W00 and the bit line D0; i.e., a transistor is not used to make a connection or contact to a word line or a bit line); the word lines divided into a number of segments (for example, BLOCK (0,0) through BLOCK (0,7) in Fig. 1), each segment comprising and being defined by a plurality of adjoining bit lines (for example, D0-D7 for BLOCK (1,0)); each word line in a segment is differentiated based on the position of the word line within the segment (i.e., in different row positions), each word line in the segment being adjoined to a separate bit line (i.e., in a matrix structure); a plurality of sensing means (for example, SA in WRC0-WRC7), each being adapted for sensing the charge flow in the bit line

connected therewith in order to determine a logical value stored in the memory cell defined by the bit line (see, for example, column 12, lines 42-54).

However, Kuroda does not disclose means for connecting each separate bit line assigned to a segment with a different associated sensing means, such that a world line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment.

Clemons, for example in Figs. 2 and 3, discloses a means (for example, via T200-T203 controlled by BYTE BLOCK DECODER) for connecting each separate bit line (for example, bit lines for columns C11-C14) assigned to a segment (for example, BYTE BLOCK 1, when selected) with a different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), such that the world line of the same position within each segment is selected within each segment (i.e., for example, a selected word line within BYTE BLOCK 1), each word line of the same position being sensed at the same time by said respective different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), thus enabling simultaneous connection of all memory cells (for example, M111 - M114) assigned to a word line (for example, R1) on a segment (for example, BYTE BLOCK 1) for readout via the corresponding bit lines (for example, bit lines for columns C11 - C14) of the segment.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kuroda by incorporating the means of Clemons for connecting each bit line assigned to a segment with an associated sensing means, thus

enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, as an equivalent alternative means for segmenting and simultaneously accessing a byte (or a word or other widths of bits) of information from the memory (compare with Fig. 1 of Clemons, which is similar to the configuration of Kuroda), for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43).

Regarding claims 14 and 16, the above Kuroda/Clemons combination further discloses that the number of sensing means is equal to the number of bit lines within each segment (for example, Figs. 2 and 3 of Clemons, as applied to the above combination, show 4 sensing means SA1-SA4 for 4 bit lines within each segment or BYTE BLOCK), where each segment contains the same number of bit lines (for example, 4 bit lines in each BYTE BLOCK in Fig. 2 of Clemons), such that each bit line in each segment (when selected) is sensed at a different sensing means (via corresponding SA1-SA4 in Fig. 3 of Clemons).

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1 above, and further in view of Dierke (U.S. Pat. No. 5,734,615).

Regarding claim 2, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claim 1 above, with the exception of the simultaneous

connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Dierke, for example in Fig. 7, discloses multiplexers (42-0' through 42-7') for simultaneously connecting (since multiplexers are commonly controlled) each bit line of a segment (three segments defined by BIT 0-7, BIT 8-15 and BIT 16-23) with an associated sensing means (at the output of each multiplexer).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the multiplexing means of Dierke for the multiplexing means of Clemons, since both means are equivalent for simultaneously connecting bit lines of a segment with an associated sensing means, for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43), and the selection of these equivalents would be within the level of ordinary skill in the art.

Regarding claims 3-5, the above Kuroda/Clemons/Dierke combination further discloses that the number of multiplexers corresponds to the largest number of bit lines defining a segment (in Fig. 7 of Dierke, eight bit lines per segment; when adapted for Clemons with four multiplexers; see Clemons, Fig. 2), each bit line of a segment being connected with a 3 multiplexer (see Dierke, Fig. 7 in which BIT 0-7, for example, are connected to the respective multiplexers); wherein the output of each multiplexer is connected with a signal sensing means (inherent in Dierke, Fig. 7; SA1-SA4 in Fig. 3 of Clemons); wherein the signal sensing means is a sense amplifier (SA1-SA4 in Fig. 3 of Clemons).

7. Claims 12, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1, 14 and 17 above, and further in view of Seyyedy (U.S. Pat. No. 5,969,380).

Regarding claims 12, 15 and 18, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claims 1, 14 and 17 above, with the exception of a volumetric data storage apparatus with a plurality of stacked layers, each layer comprising one of said non-volatile passive matrix memory devices. Seyyedy, for example in Figs. 1 and 2, discloses a ferroelectric volumetric data storage apparatus with a plurality of stacked layers (for example, four layers in Fig. 1 and three layers in Fig. 2), each layer comprising one of non-volatile passive matrix memory devices (planar ferroelectric memory arrays). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to stack a plurality of devices (as discloses in the above combination of Kuroda and Clemons) in a volumetric data storage apparatus, as in Seyyedy, for the purpose of increasing the density of memory cells over a given substrate area.

Response to Arguments

8. Applicant's arguments filed 31 October 2007 have been fully considered but they are not persuasive.

Examiner generally acknowledges Applicant's explanation of *inter alia* the differences between a "passive" matrix and an "active" matrix, starting at the bottom of page 2 through the top half of page 4; Applicant's explanation of the present invention, starting at the bottom half of

page 4 through page 5; and Applicant's characterization of the Kuroda and Clemons references, starting at the bottom of page 5 through the middle of page 8.

Specifically, in response to Applicant's argument, in the bottom paragraph on page 7, that Clemons "is not at all concerned with ferroelectric or electret memories, but rather a semiconductor SRAM memory" (a similar argument is presented staring at the bottom of page 9) and that "at least what could be termed multiplexing arrangement of Clemons cannot be adapted to a memory of Kuroda," it is note that Clemons was cited as a secondary reference that discloses a bit line selection (or multiplexing) means for simultaneously selecting all the bit lines in a column block (or a word line segment), which a person of ordinary skill in the art would recognize as being applicable to various types of memory with an array of memory cells with word lines and bit lines, including the memory of Kuroda.

Further, as indicated in the previous Office Action, the bit line selection means in Fig. 1 of Kuroda (Y-SELECT 0 through Y-SELECT 7), in which one bit line in each column block is selected for the respective I/O circuit (WRC0-WRC7), is similar to the bit line selection means in the "prior art" Fig. 1 of Clemons (T100-T111), in which one bit line in each column block is selected for the respective I/O circuit (I/O1-I/O4). Since the embodiment in Figs. 2 and 3 of Clemons was disclosed as an improvement over the "prior art" embodiment in Fig. 1 of Clemons (with a bit line selection means that is similar to that in Fig. 1 of Kuroda, as discussed above), one of ordinary skill in the art would be motivated, in view of Clemons, to modify the bit line selection means in Fig. 1 of Kuroda in a manner similar to that in Fig. 2 of Clemons (without an undue increase in complexity and/or voltage stress), in order to attain a similar improvement/

benefit for the memory of Kuroda. Thus, when Kuroda and Clemons are combined as such, the combination would include all the limitations as claimed. See the previous rejections, repeated above.

In response to Applicant's argument with respect to the Seyyedy reference, near the bottom of page 8, it is noted that the Seyyedy reference was cited as a secondary reference exemplifying a volumetric memory architecture that provides an increased storage density per area. See the previous rejections, repeated above.

In response to Applicant's argument with respect to the Dierke reference, starting at the bottom of page 8, it is noted that one of ordinary skill in the art will recognize the equivalence between the multiplexing means of Dierke and that of Clemons and would substitute one for the other as equivalent alternatives. See the previous rejections, repeated above.

Regarding Applicant's "Response to Examiner's Comments" starting in the middle of page 9, see the clarifications above.

Conclusion

9. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114.

See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) H. Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

/J. H. Hur/
Primary Patent Examiner
Art Unit 2824
26 December 2007